Department of ECM **PVP12**

4/4 B.Tech. EIGHTH SEMESTER
ELECTIVE – IV

EM8T3A **ASIC DESIGN** **Credits: 3**

Lecture: 3 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks**

Course objectives :

• To learn the advanced concepts of modern VLSI circuit and system design, including differences between ASICs and FPGAs, standard cells, cell libraries, IPs etc.

Outcome:

After completing this course, the student would have gained

- knowledge CMOS logic cells and Programming of ASIC
- Design of ASIC

UNIT I

Introduction to ASICs: Types of ASICs, Design flow, Case study, Economics of ASICs, ASIC cell library

UNIT II

CMOS logic cells: Combinational logic cells, Sequential Logic cells, Datapath Logic cells, I/O cells, Cell compilers

UNIT III

ASIC Library Design: Transistor as resistors, Transistor as parasitic capacitance, Logic Effort, library cell design, library architecture

UNIT IV

Gate Design: Gate array cell design, standard cell design, datapath cell design

UNIT VI

Programmable ASICs: Antifuse, Static RAM, EPROM, EEPROM technology, Practical issues

UNIT VII

Programmable ASIC I/O cells and iterconnect: DC output, AC output, DC input, AC input, Clock input, Power input, Xilinx I/O Block Actel ACT routing resources, emlore's constant,

UNIT VIII

Delay :RC delay in antifuse connections, antifuse parasitic capacitance

Reference Books:

1. Michael John Sebastin Smith, - "Application - Specific Integrated Circuits" – Pearson Education, 2003
2. Malcolm R.Haskard; Lan. C. May, "Analog VLSI Design - NMOS and CMOS" Prentice Hall, 1998.
3. Andrew Brown, - "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991.
4. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "Field Programmable Gate Arrays"- Kluwer Academic Publishers, 1992.